REMARKS

Claims 5, 7, 8, 11, 15, 16, 19, 20, 31 and 37 have been amended. Claims 1-39 are pending in the application. Reconsideration of the application is requested in view of the amendments and the remarks to follow.

Claims 5, 7, 8, 11, 15, 16, 19, 20, 31 and 37 have been amended to correct minor informalities and/or to respond to the concerns noted in the Office Action (pages 2 and 3), however, these amendments are not intended to alter the scope of the claims.

Allowable Subject Matter:

The Office Action is silent with respect to claims 5-8, 10-12, 15, 16, 18-20, 22-24, 26, 28-30, 32, 33 and 35-39, other than a blanket statement on page 5 to the effect that "Claims 5-8, 10-12, 15, 16, 18-20, 22-24, 26, 28-30, 32, 33, 35-39 are rejected on the same ground [sic] as stated above." The Office Action is silent with respect to claims 9, 14, 17, 21, 27 and 34, other than a blanket statement on page 7 to the effect that "Claims 9, 14, 17, 21, 27 and 34 are rejected on the same ground [sic] as stated above." This provides Applicant with no capability for meaningful response with respect to any of claims 5-12, 14-25, 27-30 and 32-39, despite citation of new art. Inasmuch as no meaningful basis for rejection is provided in the Office Action, Applicant assumes that these claims are allowable over the art of record. In the event that the Examiner finds such claims to be not allowable, a subsequent non-final Office Action should made with a clearly-stated basis for such newly-presented grounds of rejection.

Claims Objected To:

The Office Action indicates (p. 2) that claims 7, 11 and 15, as filed, have suddenly become objected to, because the Office Action now alleges that their forms are improper. Applicant is puzzled, because, not only has the present application been through no less that three prior Office Actions and Responses, all with the SAME Examiner, but also the claim formats are similar to those of many issued U.S. Patents. The Office Action provides no authority for this sudden change of posture by the USPTO.

However, in the spirit of cooperation and in order to advance the prosecution of the application, claims 7, 11 and 15 have been amended to place them in independent form. Claims 7, 11 and 15, as presented as amended, comport with appropriate claim drafting practice in conformance with patent practice appropriate to the United States of America.

Rejection Under 35 U.S.C. §112:

Claims 5-11, 16-23, 31 and 37-39 stand rejected under 35 U.S.C. 35 U.S.C. §112, second paragraph, on indefiniteness grounds. Claims 5, 7, 8, 11, 16, 19, 20, 31 and 37 have been amended to obviate the concerns noted in the Office Action, however, these amendments are not intended to alter the scope of the claims.

The Examiner is reminded of the obligation to avoid piecemeal examination, as set forth in MPEP §707.07(g), entitled "Piecemeal Examination". This MPEP section states that:

> Piecemeal examination should be avoided as much as possible. The examiner ordinarily should reject each claim on all valid grounds available, avoiding, however, undue multiplication of references. (See MPEP §904.03.) Major technical rejections on grounds such as lack of proper disclosure, lack of enablement, serious indefiniteness and res judicata should be applied where appropriate even though there may be a seemingly sufficient rejection on the basis of prior art. Where a major technical rejection is proper, it should be stated with a full development of reasons rather than by a mere conclusion coupled with some stereotyped expression.

Accordingly, in the interests of compact prosecution, Applicant respectfully requests that the Office undertake to provide all grounds of rejection as early as is practicable in prosecution. Applicant also respectfully requests that any such rejection be fully articulated in a meaningful fashion that permits a reasonable response to be timely tendered thereto.

Rejection under 35 U.S.C. §103:

The Office Action states (page 3) that claims 1, 2, 4-8, 10-13, 15, 16, 18-20, 22-26, 28-30, 32, 33 and 35-39 stand rejected under 35 U.S.C. 35 U.S.C. §103(a) over Christie et al., U.S. Patent No. 6,230,259 B1 (hereinafter "Christie"), in view of Rosenthal et al., U.S. Patent No. 5,918,050 (hereinafter "Rosenthal"). The Office Action states (p. 6) that claims 3, 9, 14, 17, 21, 27, 31 and 34 stand rejected over Christie in view of Rosenthal and further in view of Applicant's admitted prior art. Applicant respectfully submits that claims 1-39 are not unpatentable over Christie and Rosenthal and/or any admitted prior art and requests reconsideration.

Christie is directed to (Title) a system using a "Transparent extended state save". Christie discloses (Abstract) that "A microprocessor having a standard register set and an extended register set, which is configured to save its state upon suspension of either an extended register process or a standard register processor. The microprocessor is configured to execute both standard register instruction sequences and extended register instruction sequences. A first memory is provided for storing a state of the microprocessor when a standard register instruction set sequence is suspended. The microprocessor further comprises a second memory for storing a microprocessor state upon suspension of the microprocessor executing an extended register instruction set sequence. An extended state save circuit coupled between a microprocessor core and the second memory allows the extended state of the microprocessor to be stored without modification of the operating system. As a result, the extended state of the microprocessor can be saved transparently to the operating system."

Rosenthal is directed to (Title) an "Apparatus accessed at a physical I/O address for address and data translation and for context switching of I/O devices in response to commands from application programs". Rosenthal states that "A computer system including a central processing unit, a system input/output bus, an input/output device, and an input/output control unit accessed at a physical input/output address for translating addresses and data in commands from applications programs to physical input/output device addresses and for changing the context of an input/output device for which an address translation is furnished." (Abstract).

The Office Action states (page 3, item 6) that "Regarding claim 1, Christie discloses in a computer device having a processor that generates a first address signal of a first width and a second address signal of a second width that is greater than the first width, wherein the second address signal is produced in the computing device by concatenating an address extension from an address extension register with the first address signal (fig. 6 and 7c, col. 12, line 10 - col. 13, line 21) ...."

First, Christie is silent regarding generation of address signals, as recited within claim 1. The passage in col. 12, line 1 et seq. of Christie is reproduced below:

> Special extended register set instructions may move **data** between the standard and extended registers. The standard registers may map to extended registers so that the standard registers can be modified when microprocessor 212 is in the extended register mode of operation. The EIP and ESP registers should map to functionally identical extended registers. This allows EIP and ESP values when the microprocessor is in standard or extended mode, to be coherent thereby facilitating interaction between the modes.

An alternative embodiment of register file 244 is shown in FIG. 7c. In the register file 244 shown in FIG. 7c, extension register set 272 includes standard register set 270. In this embodiment, the standard register set 270 forms the least significant registers of register file 244. Alternatively the standard registers may form the lower portions of the least significant registers of register file 244. Extension register set 272 includes all of the registers contained within standard register 270 and the additional register sets shown in FIG. 7c as the registers 272 n+1 to register 272 m. The embodiment of register file 244 shown in FIG. 7c advantageously minimizes the number of registers required. If, for example, standard register set 270 comprises 8 registers and extension register set 272 includes 32 registers, then 40 registers would be required in the embodiment of register file 244 shown in FIG. 6 whereas only 32 registers, are required to implement the register file architecture shown in FIG. 7c. The architecture of register file 244 shown in FIG. 7c results in a correspondence between the registers of standard register set 270 and the least significant registers of extension register set 272. The correspondence between the registers of standard register set 270 and a portion of the extension register set 272 provides an architecture in which the addressing of extension register set 272 may be accomplished by simply concatenating additional bits onto the standard register reference field used to address standard register set 270.

This concatenation of register addressing bits is implemented in the embodiment of the present invention used with the microprocessor instruction 250 shown in FIG. 7a. A typical microprocessor instruction 250 of the present invention includes a first and a second register reference. In a typical instruction, the first register reference may be the source register providing the information (or the address of the memory location containing the information) that will be manipulated by the particular microprocessor operation. The second register reference provides a target register (or the address of a target memory location) to which the manipulated information will be ultimately stored. In an extended register set microprocessor, it is required that the extension register set is available both as a target or source register and as a destination register. To accommodate the first and second register references and the extension register set, the present invention contemplates that microprocessor instructions which require use of the extension register set will signify to the microprocessor with the extension register key field described previously. The instruction decode unit is configured to interpret an additional byte appended to the mod r/m byte of the microprocessor instruction when extension register key field 252 contains the extension register key value. The additional byte appended to the microprocessor instruction contains, in a presently preferred embodiment, a 5 bit field for the second extension register reference and a 2 bit first register field that is concatenated with a three bit first

register field of the mod r/m byte of the microprocessor instruction. Turning to FIG. 7a, two bytes of a microprocessor instruction 250 are shown. The first or mod r/m byte of microprocessor instruction 250 includes a two bit mod field, a three bit first register reference field 284, and the extended register key field 252 as described previously. Assuming for purposes of this example that the extension register key value is 1-0-0, then an additional byte is appended to mod r/m byte of microprocessor instruction 250 if extended register key field 252 equals 1-0-0. The additional byte appended to mod rim byte of microprocessor instruction 250 includes a 5 bit second register reference field 282 and a 2 bit extended first register reference field 200. The two bits of extended first register reference field 280 are appended or concatenated to the 3 bit first standard reference field 284 in the mod r/m byte so that the two-bit field 280 forms the most significant bits of the 5-bit concatenated field. The 5 bit second register field 282 contains the information necessary to identify one of the selected extension register sets. It will be appreciated to those skilled in the art of microprocessor architecture and programming that the 3-bit fields associated with the standard register references typically imply a register set comprising a maximum of eight registers whereas the 5 bit field of the extension register set implies a maximum of 32 registers.

Thus, instruction decode unit 238 in one embodiment is configured to receive a microprocessor instruction 250 that includes a first register reference and a second register reference. The first register reference and a second reference are indicative of first and second selected registers respectively. Microprocessor instruction 250 further includes operating mode information that is indicative of whether the instruction decode unit 238 is operating in a standard register mode or an extension register mode. In one embodiment, the operating mode information may simply comprise the extended register key field 252. If the extended register key field 252 contains an extended register key value, then instruction decode unit 238 is operating in an extension register mode and instruction decode unit 238 is configured to access the contents of first and second selected registers in response to receiving the microprocessor instruction 250. The first and second registers a relocated within the standard register set 270 if the instruction decode unit is operating in a standard register mode whereas the first and second selective registers are located within the extension register set 272 when instruction decode unit 238 is operating in extension register mode.

This passage describes addressing schemes for an extended register set, i.e., addressing that is completely internal to the computer, with the extended register set being employed to store **data**.

Second, the reason Christie provides for having such an extended register set is to be able to save the internal state of the computer upon suspension of a register process (see, e.g., Abstract, Field of the Invention, col. 2, line 6 et seq., Summary, etc.). Accordingly, modifying the teachings of Christie to arrive at the subject matter recited in Applicant's claims renders the teachings of Christie unsuitable for their intended purpose. It is improper to employ a reference in a manner that renders the teachings of the reference unsuitable for their intended purpose, as is explained below in more detail with reference to MPEP §2143.01, entitled "Suggestion or Motivation To Modify the References".

This MPEP section states, in a subsection entitled "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE", that "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)".

The cited passages are void of the teachings for which they are quoted. Christie teaches use of bus bridges for generation of address signals for peripheral devices, stating (col. 5, line 43 et seq.) that:

> Bus bridge 218 is configured to effect communications between I/O devices 220, main memory 216, and microprocessor 212. It is noted that system bus 224 and CPU bus 222 are typically high bandwidth, high speed buses to allow large amounts of data to be transferred between microprocessor 212, external cache 214, and main memory 216. I/O devices 220 are typically devices which do not require such

> high bandwidth, and may not be capable of the high frequency switching of system bus 224 and CPU bus 222. Bus bridge 218 therefore provides a buffer between I/O bus 226 (typically a lower speed, lower bandwidth bus than system bus 224 and CPU bus 222) and system bus 224. Additionally, system bus 224 and CPU bus 222 may employ a different bus protocol than I/O bus 226. Bus bridge 218 provides a translation between the different protocols. In one embodiment, I/O bus 226 is a Peripheral Component Interconnect (PCI) bus. In another embodiment, I/O bus 226 is an Industry Standard Architecture (ISA) bus. In still another embodiment, I/O bus 226 is an Enhanced ISA (EISA) bus. Different embodiments of bus bridge 218 may be used for the different embodiments of I/O bus 226. Additional bus bridges similar to bus bridge 218 may be attached to system bus 224 and/or I/O bus 226.
>
> I/O devices 220 are configured to effect communications between computer system 210 and other devices coupled thereto. For example, I/O devices 220 may include a serial or parallel card for connecting devices such as printers or external modems to computer system 210. Additional I/O devices 220 may include a modem, a sound card, a network adapter, etc. I/O devices 220 typically include at least one storage device as well. Storage devices may be hard disk drives, floppy disk drives, and compact disk, read-only-memory (CD-ROM) drives. It is noted that I/O devices 220 may also be referred to as peripheral devices.
>
> It is noted that CPU bus 222 and system bus 224 may be configured according to the same bus protocol or, alternatively, to different bus protocols. Many varied bus protocols are well known, and any bus protocol may be suitable for CPU bus 222 and system bus 224. It is further noted that, although FIG. 4 shows a computer system 210 including a single microprocessor 212, other embodiments of computer system 210 including multiple processors are contemplated. Such embodiments may include multiple processors coupled to an external cache, multiple processors coupled to multiple external caches, or multiple processors coupled to system bus 224.

Indeed, a similar prior art system is described in Applicant's specification (see, e.g., p. 2, line 12 et seq.; p. 3, line 22 et seq. describes the problems which the subject matter recited in Applicant's claims resolves in a multitasking environment). Christie is concerned with saving a state of a processor during one operation when that operation is suspended to undertake another operation and is silent with respect to use of extended registers for addressing of peripheral

devices, as recited in each of Applicant's independent claims 1, 5, 8, 12, 16, 20, 24, 33 and 37.

In contrast to Christie and/or the subject matter of any of Applicant's claims, Rosenthal teaches (col. 10, line 55 et seq.) that:

> In order to achieve all of these improvements, the present invention utilizes an architecture illustrated in block diagram in FIG. 2. As may be seen, although the input/output architecture may be used with systems utilizing a single input/output bus for all operations, the architecture functions as well in a system 22 utilizing a local bus 27 such as the Peripheral Component Interconnect (PCI) bus or the Video Electronics Standards Association (VESA) local bus which may be associated with other input/output buses. While the discussion of this particular figure will assume that the bus 27 is a PCI bus, the local bus 27 is also referred to in this specification as the input/output bus 27. In arrangements utilizing local buses, the central processing unit 21 and main memory 23 are typically arranged on a processor bus 24 and a memory bus 26, respectively, and are joined to a bridge unit 25. The central processing unit 21 typically includes a memory management unit such as that described above. The bridge unit 25 provides write buffering for operations between the central processing unit 21 and the input/output bus 27, between the central processing unit 21 and main memory 23 on the processor bus 24 and the memory bus 26, and between the input/output bus 27 and main memory 23.
>
> Typically, various input/output devices are arranged on the input/output bus 27 as bus masters and bus slaves. In prior art systems, these local bus masters and slaves are those components (such as a graphics output device for connecting an output display monitor, a local area network, or a hard disk controller unit) which require the most rapid input/output operations for system success. If such local bus masters and slaves are connected to the input/output bus 27, they are utilized with the present architecture for the purpose of running legacy programs and input/output functions not implemented by the input/output control unit 29.
>
> In the new architecture, a single input/output control unit 29 is shown joined to the input/output bus 27. The control unit 29 includes a hardware FIFO unit 31 for receiving incoming commands addressed to the input/output devices on a device bus 34. In this embodiment of the invention, only a single FIFO unit 31 is used although a plurality of FIFO buffers might be used at greater expense in order to further accelerate operations. The unit 29 receives physical addresses on the input/output bus 27 furnished by

> the system memory management unit and virtual names furnished by application programs for operations to be performed at the FIFO unit 31 and controls the translation of those addresses and virtual names into physical addresses and context for all the associated input/output devices. The hardware unit 29 includes the device bus 34 to which the individual input/output devices such as a disk controller 32, a graphics output controller 33, and a sound generator 37 are shown joined. The unit 29 also includes a DMA unit 35 which is adapted to transfer data between the individual input/output devices and main memory for use by the central processing unit or other components of the system.

Applicant further notes that Christie and Rosenthal are void of any mention of any "thread", as recited in each of Applicant's independent claims 1, 5, 8, 12, 16, 20, 24, 33 and 37. As a result, it is inconceivable that these references could teach, disclose, suggest or motivate "concurrently executing threads of a plurality of application programs, wherein different ones of the threads indicate one or more address extensions to an operating system", as recited in claim 1 or as alleged in the Office Action (page 4).

Christie is concerned with saving processor state data in extension registers. Rosenthal is concerned with physical address translation in a multitasking environment, and teaches use of a bridge unit for addressing a peripheral I/O bus. These are completely different areas of endeavor than that contemplated by Applicant.

There is no motivation in either of the references to modify their teachings to provide a peripheral addressing scheme such as is recited in Applicant's claims because each of the references teaches at least one specific type of peripheral addressing scheme that is different from the subject matter of Applicant's claims. Additionally, the Office Action states that "it would have been obvious ...." to modify the teachings of Christie and/or Rosenthal. However, this unsupported conclusion does not reflect the test for unpatentability.

With respect to all such allegations, as there is no basis for the Examiner's contentions within the cited reference, the only possible motivation for these contentions is hindsight reconstruction wherein the Examiner is utilizing Applicant's own disclosure to construct a reason for modifying the cited reference. The Examiner is reminded that hindsight reconstruction is not an appropriate basis for a §103 rejection. (*See, e.g., Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990) (explaining that hindsight reconstruction is an improper basis for rejection of a claim).) Such an ad hoc conclusion also fails to provide evidence of motivation or suggestion to modify (see *In re Dembiczak*, infra).

Further, there is no basis for the Examiner's contentions within the cited reference. No motivation is identified in the reference for the proposed modification and additions to the disclosure of the reference. Moreover, no evidence to motivate modification of the reference is identified. Against this backdrop, the rejection clearly employs an improper 'obvious to try' standard for finding unpatentability (discussed infra).

Applicant notes the requirements of MPEP §2143, entitled "Basic Requirements of a Prima Facie Case of Obviousness" (see also MPEP §706.02(j), entitled "Contents of a 35 U.S.C. 103 Rejection."). MPEP §2143 states that "To establish a prima facie case of obviousness, three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." Inasmuch as the reference fails to teach or disclose the elements recited in the claims, the reference

cannot provide motivation to modify their teachings to arrive at the invention as claimed, and the Examiner has identified no such teaching or disclosure in the reference. As a result, the first prong of the test cannot be met.

MPEP §2143 further states that "Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Inasmuch as the reference fails to provide all of the features recited in Applicant's claims, as set forth with particularity hereinabove, the third prong of the test is not met. As a result, there cannot be a reasonable expectation of success. As such, the second prong of the test cannot be met.

MPEP §2143 additionally states that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." This fourth criterion cannot be met because the reference fails to teach or disclose the elements recited in the claim.

In fact, Christie is directed solely to techniques for transparently saving a state of a processor, while Rosenthal is directed solely to I/O mapping in a multitasking environment. The claimed subject matter addresses a broader range of issues including accession of peripheral devices and does so in a fundamentally different way. There is no motivation or suggestion in Christie or Rosenthal to even consider the problems addressed by the instant disclosure, and no guidance whatsoever to point the artisan towards the claimed subject matter.

No guidance has been identified within the reference to determine which elements to pick or choose from the reference, or of how to couple them to

somehow arrive at subject matter such as is claimed. Accordingly, the unpatentability rejections fail all of the criteria for establishing a prima facie case of obviousness as set forth in the MPEP.

There is no teaching or guidance identified within the references to aid one of ordinary skill in picking and choosing elements from the diverse embodiments of the references or in assembling those elements to attempt to arrive at the subject matter of any of Applicant's claims. As such, the rejection employs an improper "obvious to try" standard of unpatentability.

Such is improper, as is discussed below in more detail with reference to MPEP §2145(X)(B), entitled "Obvious To Try Rationale". This MPEP section states that "The admonition that 'obvious to try' is not the standard under §103 has been directed mainly at two kinds of error. In some cases, what would have been 'obvious to try' would have been to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful. In others, what was 'obvious to try' was to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it." *In re O'Farrell*, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988) (citations omitted)".

In this instance, no guidance in selecting some but not others of the elements described within the teachings of the references is identified. Similarly,

no direction as to which of many possible choices is likely to be successful has been identified.

As there is no basis for the Examiner's contentions within the cited references, the only possible motivation for these contentions is hindsight reconstruction wherein the Examiner is utilizing Applicant's own disclosure to construct a reason for combining and/or modifying the teachings of the cited references. The Examiner is reminded that hindsight reconstruction is not an appropriate basis for a §103 rejection. (See, e.g., *Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990) (explaining that hindsight reconstruction is an improper basis for rejection of a claim).)

Moreover, with respect to all of the unpatentability rejections, no evidence has been provided as to why it would be obvious to modify the teachings of the reference. Evidence of a suggestion to combine or modify may flow (i) from the prior art reference itself, (ii) from the knowledge of one skilled in the art or (iii) from the nature of the problem to be solved. However, this range of sources does not diminish the requirement for actual evidence. Further, the showing must be clear and particular. See *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

For at least these reasons, Applicant respectfully requests that the §103 rejections be withdrawn, and that Applicant's claims 1-39 be allowed.

Conclusion

To recapitulate, Applicant has pointed out that (i) the Office Action fails to provide meaningful grounds for rejection of many of Applicant's claims, (ii) the references do not provide the claimed subject matter, (iii) the references are rendered unsuitable for their intended purposes in attempting to modify their teachings to arrive at the claimed subject matter, (iv) the rejection fails to meet the standards set forth in the MPEP for a finding of unpatentability, (v) there is no motivation to modify the teachings of the references, (vi) the rejection appears to employ hindsight reconstruction, (vii) the rejection appears to use an improper 'obvious to try' standard for finding unpatentability, (viii) there is no teaching or guidance in the references to suggest the claimed subject matter and (ix) the references fail to provide any evidence of motivation to combine.

Claims 1-39 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

Date: Aug. 13, 2004

By: _____

Frederick M. Fliegel
Reg. No. 36,138
(509) 324-9256 x239